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**1** [Pointer cache assisted prefetching](#)

Jamison Collins, Suleyman Sair, Brad Calder, Dean M. Tullsen

 November 2002 **MI CRO 35**: Proceedings of the 35th annual ACM/IEEE inter Microarchitecture

**Publisher:** IEEE Computer Society Press

 Full text available: [Publisher Site](#), [Pdf \(1.21 MB\)](#) Additional Information: [full citation](#), [terms](#)
**Bibliometrics:** Downloads (6 Weeks): 2, Downloads (12 Months): 40, Citation

Data prefetching effectively reduces the negative effects of long load lat modern processors. Hardware prefetchers employ hardware structures i addresses based on previous patterns. Thread-based prefetchers ...

**2** [Speculative execution in a distributed file system](#)

Edmund B. Nightingale, Peter M. Chen, Jason Flinn

 October 2005 **SOSP '05**: Proceedings of the twentieth ACM symposium on

**Publisher:** ACM [Request Permissions](#)

 Full text available: [Pdf \(305.54 KB\)](#) Additional Information: [full citation](#), [abstract](#), [review](#)
**Bibliometrics:** Downloads (6 Weeks): 11, Downloads (12 Months): 164, Citatio

Speculator provides Linux kernel support for speculative execution. It al share speculative state by tracking causal dependencies propagated thr communication. It guarantees correct execution by preventing ...

**Keywords:** causality, distributed file systems, speculative execution

Also published in:

 October 2005 **SIGOPS Operating Systems Review** Volume 39 Issue 5

**3** [Speculative execution in a distributed file system](#)

Edmund B. Nightingale, Peter M. Chen, Jason Flinn

 November 2006 **Transactions on Computer Systems (TOCS)** , Volume 24 I

**Publisher:** ACM [Request Permissions](#)

 Full text available: [Pdf \(1.11 MB\)](#) Additional Information: [full citation](#), [abstract](#), [review](#)
**Bibliometrics:** Downloads (6 Weeks): 7, Downloads (12 Months): 116, Citatio

Speculator provides Linux kernel support for speculative execution. It al

share speculative state by tracking causal dependencies propagated through communication. It guarantees correct execution by preventing speculation.

**Keywords:** Distributed file systems, causality, speculative execution

#### 4 Rethink the sync

 Edmund B. Nightingale, Kaushik Veeraraghavan, Peter M. Chen, Jason Flinn  
September 2008 **Transactions on Computer Systems (TOCS)**, Volume 26

**Publisher:** ACM  [Request Permissions](#)

Full text available:  Pdf (387.05 KB) Additional Information: [full citation](#), [abstract](#), [rss](#)

**Bibliometrics:** Downloads (6 Weeks): 14, Downloads (12 Months): 382, Citation


We introduce *external synchrony*, a new model for local file I/O that provides simplicity of synchronous I/O, yet also closely approximates the performance of an external observer cannot distinguish the output ...

**Keywords:** File systems, causality, speculative execution, synchronous

#### 5 A compiler framework for speculative optimizations

 Jin Lin, Tong Chen, Wei-Chung Hsu, Pen-Chung Yew, Roy Dz-Ching Ju, Tin  
September 2004 **Transactions on Architecture and Code Optimization**

**Publisher:** ACM  [Request Permissions](#)


Full text available:  Pdf (466.65 KB) Additional Information: [full citation](#), [abstract](#), [rss](#)

**Bibliometrics:** Downloads (6 Weeks): 9, Downloads (12 Months): 73, Citation

Speculative execution, such as control speculation or data speculation, improves program performance. Using edge/path profile information or simple heuristics, the frameworks can adequately incorporate and exploit ...

**Keywords:** Data speculation, partial redundancy elimination, register pressure, speculative weak update

#### 6 The Jrpm system for dynamically parallelizing Java programs

 Michael K. Chen, Kunle Olukotun  
June 2003 **ISCA '03: Proceedings of the 30th annual international symposium on computer architecture**

**Publisher:** ACM

Full text available:  Pdf (320.42 KB) Additional Information: [full citation](#), [abstract](#), [rss](#)


**Bibliometrics:** Downloads (6 Weeks): 8, Downloads (12 Months): 65, Citation

We describe the Java runtime parallelizing machine (Jrpm), a complete framework for parallelizing sequential programs automatically. Jrpm is based on a chip multiprocessor architecture (TLS) support. CMPs have low sharing and communication ...

Also published in:

May 2003 **SIGARCH Computer Architecture News** Volume 31 Issue 2

#### 7 A cost-driven compilation framework for speculative parallelization of

-  Zhao-Hui Du, Chu-Cheow Lim, Xiao-Feng Li, Chen Yang, Qingyu Zhao, Tin-June 2004 **PLDI '04**: Proceedings of the ACM SIGPLAN 2004 conference on design and implementation

**Publisher:** ACM  [Request Permissions](#)

Full text available:  [Pdf](#) (235.14 KB) [Additional Information: full citation, abstract, etc.](#)


**Bibliometrics:** Downloads (6 Weeks): 16, Downloads (12 Months): 99, Citation

The emerging hardware support for thread-level speculation opens new sequential programs beyond the traditional limits. By speculating that n unlikely during runtime, consecutive iterations of a sequential ...

**Keywords:** cost-driven compilation, loop transformation, speculative m parallel threading, speculative parallelization, thread-level speculation

Also published in:

June 2004 **SIGPLAN Notices** Volume 39 Issue 6

- 8 [Bloom filtering cache misses for accurate data speculation and prefetching](#)  
 Shih-Kwon Peir, Shih-Chang Lai, Shih-Lien Lu, Jared Stark, Konrad Lai  
June 2002 **ICS '02**: Proceedings of the 16th international conference on S


**Publisher:** ACM  [Request Permissions](#)

Full text available:  [Pdf](#) (248.57 KB) [Additional Information: full citation, abstract, etc.](#)

**Bibliometrics:** Downloads (6 Weeks): 3, Downloads (12 Months): 60, Citation

A processor must know a load instruction's latency to schedule the load the correct time. Unfortunately, modern processors do not know this lat dependent instructions should have been scheduled to ...

**Keywords:** bloom filter, data cache, data prefetching, data speculation

- 9 [Dynamic performance tuning for speculative threads](#)  
 Yangchun Luo, Venkatesan Packirisamy, Wei-Chung Hsu, Antonia Zhai, Nik June 2009 **ISCA '09**: Proceedings of the 36th annual international symposium on computer architecture

**Publisher:** ACM  [Request Permissions](#)

Full text available:  [Pdf](#) (460.67 KB) [Additional Information: full citation, abstract, etc.](#)

**Bibliometrics:** Downloads (6 Weeks): 99, Downloads (12 Months): 99, Citation


In response to the emergence of multicore processors, various novel architectures have been introduced to fully utilize these processors. One such architecture is Level Speculation (TLS), which allows potentially dependent ...

**Keywords:** dynamic optimization, multicore, parallelism, thread-level speculation




Also published in:

June 2009 **SIGARCH Computer Architecture News** Volume 37 Issue 3

- 10 [Predictor-directed stream buffers](#)


-  Timothy Sherwood, Suleyman Sair, Brad Calder  
December 2000 **MICRO 33**: Proceedings of the 33rd annual ACM/IEEE inter  
Microarchitecture

**Publisher:** ACM

Full text available:  [Publisher Site](#),  [Pdf](#) (187.89 KB),  [Ps](#) (1.12 MB) [Additional Info](#)

**Bibliometrics:** Downloads (6 Weeks): 4, Downloads (12 Months): 45, Citation

# 11 [Early load address resolution via register tracking](#)

-  Michael Bekerman, Adi Yoaz, Freddy Gabbay, Stephan Jourdan, Maxim Kal  
June 2000 **ISCA '00**: Proceedings of the 27th annual international sympos  
architecture

**Publisher:** ACM

Full text available:  [Pdf](#) (143.17 KB) [Additional Information: full citation, abstract, re](#)


**Bibliometrics:** Downloads (6 Weeks): 2, Downloads (12 Months): 32, Citation

Higher microprocessor frequencies accentuate the performance cost of i  
especially noticeable in the Intel's IA32 architecture where lack of regist  
number of memory accesses. This paper presents novel, ...

Also published in:

May 2000 **SIGARCH Computer Architecture News** Volume 28 Issue 2

# 12 [Unbounded page-based transactional memory](#)

-  Weihaw Chuang, Satish Narayanasamy, Ganesh Venkatesh, Jack Sampson  
Gilles Pokam, Brad Calder, Osvaldo Colavin  
November 2006 **ASPLOS-XII**: Proceedings of the 12th international confere  
for programming languages and operating systems

**Publisher:** ACM 

Full text available:  [Pdf](#) (242.68 KB) [Additional Information: full citation, abstract, re](#)

**Bibliometrics:** Downloads (6 Weeks): 8, Downloads (12 Months): 102, Citation

Exploiting thread level parallelism is paramount in the multicore era. Tr  
programmers to expose such parallelism by greatly simplifying the mult  
model. Virtualized transactions (unbounded in space and time) are ...

**Keywords:** concurrency, parallel programming, transactional memory,


Also published in:

October 2006 **SIGOPS Operating Systems Review** Volume 40 Issue 5

October 2006 **SIGARCH Computer Architecture News** Volume 34 Issue 5

November 2006 **SIGPLAN Notices** Volume 41 Issue 11

# 13 [InvisiFence: performance-transparent memory ordering in conventio](#)

-  Colin Blundell, Milo M.K. Martin, Thomas F. Wenisch  
June 2009 **ISCA '09**: Proceedings of the 36th annual international sympos  
architecture

**Publisher:** ACM 

Full text available:  [Pdf](#) (496.89 KB) [Additional Information: full citation, abstract, re](#)

**Bibliometrics:** Downloads (6 Weeks): 63, Downloads (12 Months): 63, Citation

A multiprocessor's memory consistency model imposes ordering constraints on atomic operations, and memory fences. Even for consistency models that allow stores, ordering constraints still induce significant ...

**Keywords:** memory consistency, parallel programming

Also published in:

June 2009 **SIGARCH Computer Architecture News** Volume 37 Issue 3

- 14 [Copy or Discard execution model for speculative parallelization on m](#)  
Chen Tian, Min Feng, Vijay Nagarajan, Rajiv Gupta  
November 2008 **MI CRO '08: Proceedings of the 2008 41st IEEE/ ACM I**  
**on Microarchitecture - Volume 00** , Volume 00

**Publisher:** IEEE Computer Society

Full text available:  Pdf (809.07 KB) Additional Information: [full citation](#), [abstract](#), [re](#)

**Bibliometrics:** Downloads (6 Weeks): 10, Downloads (12 Months): 48, Citation

The advent of multicores presents a promising opportunity for speeding up profile-based speculative parallelization of these programs. In this paper we describe an efficiently supporting software speculation on ...

- 15 [Software thread-level speculation: an optimistic library implementation](#)  
Cosmin E. Oancea, Alan Mycroft

May 2008 **IWMSE '08: Proceedings of the 1st international workshop on**  
**engineering**

**Publisher:** ACM

Full text available:  Pdf (242.51 KB) Additional Information: [full citation](#), [abstract](#), [re](#)

**Bibliometrics:** Downloads (6 Weeks): 5, Downloads (12 Months): 102, Citation

Software thread level speculation (TLS) solutions tend to mirror the hardware solutions they employ one, exact dependency-tracking mechanism. Our perspective is, perhaps, better exploited by a family of lighter, ...


**Keywords:** template metaprogramming, thread-level speculation (TLS)

- 16 [ECMon: exposing cache events for monitoring](#)

Vijay Nagarajan, Rajiv Gupta

June 2009 **ISCA '09: Proceedings of the 36th annual international symposium on**  
**architecture**

**Publisher:** ACM 

Full text available:  Pdf (1.31 MB) Additional Information: [full citation](#), [abstract](#), [re](#)

**Bibliometrics:** Downloads (6 Weeks): 51, Downloads (12 Months): 51, Citation

The advent of multicores has introduced new challenges for programme performance and software reliability. There has been significant interest in software speculation to better utilize the computational power ...

**Keywords:** cache events, recording for replay, speculation past barrier

Also published in:


June 2009 **SIGARCH Computer Architecture News** Volume 37 Issue 3

**17** [A novel approach to parenting in functional program evaluation](#)

Julian R. Dermoudy

February 2003 **ACSC '03: Proceedings of the 26th Australasian compu**  
**Volume 16**, Volume 16

**Publisher:** Australian Computer Society, Inc.

Full text available:  [Pdf](#) (86.13 KB) Additional Information: [full citation](#), [abstract](#), [re](#)

**Bibliometrics:** Downloads (6 Weeks): 0, Downloads (12 Months): 4, Citation C

The ability for multiple threads to enter the same graph node without or necessary component of the graph reduction of functional languages sin shared. Shared closures, however, compound the difficulty ...

**Keywords:** concurrency, distributed systems, functional programming

**18** [Scheduling speculative tasks in a compute farm](#)

David Petrou, Garth A. Gibson, Gregory R. Ganger

November 2005 **SC '05: Proceedings of the 2005 ACM/IEEE conference on S**

**Publisher:** IEEE Computer Society

Full text available:  [Pdf](#) (670.34 KB) Additional Information: [full citation](#), [abstract](#), [re](#)

**Bibliometrics:** Downloads (6 Weeks): 2, Downloads (12 Months): 11, Citation

Users often behave speculatively, submitting work that initially they do computing often consists of single node speculative tasks issued by, e.g dna sequences and computer graphics artists rendering ...



**19** [Memory forwarding: enabling aggressive layout optimizations by que data relocation](#)



Chi-Keung Luk, Todd C. Mowry

May 1999 **ISCA '99: Proceedings of the 26th annual international sympos architecture**

**Publisher:** ACM

Full text available:  [Publisher Site](#),  [Pdf](#) (196.77 KB) Additional Information: [full citatio](#)  
[index terr](#)

**Bibliometrics:** Downloads (6 Weeks): 4, Downloads (12 Months): 27, Citation

By optimizing data layout at run-time, we can potentially enhance the p actively creating spatial locality, facilitating prefetching, and avoiding ce sharing. Unfortunately, it is extremely difficult to guarantee ...

Also published in:

May 1999 **SIGARCH Computer Architecture News** Volume 27 Issue 2

**20** [SableSpMT: a software framework for analysing speculative multithr](#)



Christopher J. F. Pickett, Clark Verbrugge

January 2006 **PASTE '05: Proceedings of the 6th ACM SIGPLAN-SIGSOFT w for software tools and engineering**

**Publisher:** ACM  [Request Permissions](#)

**Full text available:**  [Pdf](#) (602.03 KB) **Additional Information:** [full citation](#), [abstract](#), [re](#)

**Bibliometrics:** Downloads (6 Weeks): 4, Downloads (12 Months): 43, Citation

Speculative multithreading (SpMT) is a promising optimisation technique for the execution of sequential programs on multiprocessor hardware. Analysis of such systems is however difficult and complex, and is typically ...

**Keywords:** java, profiling, speculative multithreading, static and dynamic speculation, virtual machines

Also published in:

January 2006 **SIGSOFT Software Engineering Notes** Volume 31 Issue 1

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